

IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 25. This sheet, which includes Fig. 25, replaces the original sheet including Fig. 25.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-7 and 10-19 are pending in this application. Claims 8 and 9 are canceled by the present response without prejudice. The drawings were objected to. Claims 10, 14, and 18 were objected to under 37 C.F.R. § 1.75(c). Claims 4, 12, and 16 were rejected under 35 U.S.C. § 112, first paragraph. Claims 8-19 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 6, and 7 were rejected under 35 U.S.C. § 103(a) as unpatentable over applicant's admitted art in view of U.S. patent 4,287,594 to Shirasaka and further in view of U.S. patent application publication 2001/0054166 to Fukuda. Claims 2-4, 8, 9, 11, 12, 15, 16, 18, and 19 were rejected under 35 U.S.C. § 103(a) as unpatentable over applicant's admitted art in view of Shirasaka in view of Fukuda as applied to claim 1, and further in view of U.S. patent 5,958,080 to Kang. Claims 5, 13, and 17 were rejected under 35 U.S.C. § 103(a) as unpatentable over applicant's admitted art in view of Shirasaka in view of Fukuda in view of Kang as applied to claim 2, and further in view of U.S. patent 6,560,734 to Whetsel.

Addressing first the objection to the drawings, that objection is traversed by the present response.

The drawings were first objected to as it was unclear what values "n" and "k" were representative of with regard to the figures. In reply to that position applicant draws attention to the specification at page 15, lines 5-17. At that portion the terms "n" and "k" are noted and described. Thus, the drawings are believed to be proper in that respect.

Moreover, a replacement Figure 25 is submitted herein that provides labels beyond the numerical numbering, as requested in the Office Action.

In view of the foregoing comments and the submission of replacement Figure 25, the drawings are believed to be proper.

Addressing now the objection to claims 10, 14, and 18, that objection is traversed by the present response.

Claims 10, 14, and 18 were noted as improper dependent claims. In reply each of claims 10, 14, and 18 is amended by the present response to be rewritten in independent form. The amendments to claims 10, 14, and 18 are believed to address the objections of those claims.

Addressing now the rejection of claims 4, 12, and 16 under 35 U.S.C. § 112, first paragraph, that rejection is traversed by the present response. First, applicant notes the features recited in claims 4, 12, and 16 are noted in the present specification at page 22, lines 7-14 as one example. As discussed in those portions in the specification data is first held in registers 11 and 11', and the data stored in those registers is initially the same. However, if data in one of the registers becomes corrupt, the data in register 11 and the data in register 11' will no longer match. In such a case, the register holding the non-corrupted data transmits the data to the register holding the corrupted data, and then the corrupted data is written over with the non-corrupted data in that register. Detection of the corruption of data is performed by the detection circuit.

Applicant submits the above-noted operation is clear from the specification and that thereby claims 4, 12, and 16 are proper under 35 U.S.C. § 112, first paragraph.

Addressing now the rejection of claims 8-19 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response.

The above-noted claims were rejected as they did not recite "a compression between the compression information ..." operation. In reply applicant believes claims 8-19 are proper as they are directed to an embodiment in the specification that detects corruption of data held in an information holding circuit based on whether or not the expected value information has changed. Specifically, claims 8-19 were directed to a second embodiment

described in the specification starting at page 13, line 6, and see also particularly page 13, lines 15-18. That embodiment did not utilize the same “compression” operation as in the first embodiment, and thus claims 8-19 as originally written were believed to be proper. Claims 8 and 9 are canceled by the present response but claims 10-19 as written are believed to be proper under 35 U.S.C. § 112, second paragraph for the foregoing reasons.

Addressing now the above-noted prior art rejections, those rejections are traversed by the present response.

The outstanding rejection first relies on the admitted prior art to disclose several claimed features including the claimed “detecting circuit”. In that respect applicant notes independent claim 1 is directed to a technology in which an information holding circuit holds information programmed in a programmable circuit, and a detecting circuit detects whether or not the data held in the information holding circuit has been accidentally corrupted.

The admitted art is directed to holding information programs in a programmable circuit, in an information holding circuit. However, applicant submits the outstanding rejection is misconstruing the admitted art as the admitted art does not disclose or suggest any detecting of whether or not data held in the information holding circuit has been accidentally corrupted. With respect to independent claim 1 the admitted art does not in fact disclose the “detecting circuit which compares the expected value information with compression information of the information compression circuit to check destruction of information held in the information holding circuit”. Applicant also notes the outstanding rejection has not pointed to any disclosure in the admitted art to meet that claim limitation.

Moreover, applicant respectfully submits no teachings in the secondary cited references to Shirasake or Fukuda cure the deficiencies in the admitted art.

Shirasake describes an output circuit with a detection circuitry and Fukuda describes a compression circuitry. However, applicant respectfully submits both Shirasake and Fukuda

differ from the claims and do not cure the deficiencies in the admitted art. Specifically, Shirasake and Fukuda are directed to an error detection performed *during testing of a memory*. In that respect Shirasake and Fukuda are directed to devices involving an external input to a memory, control of the memory, or addresses of the memory.

Independent claim 1, in contrast to Shirasake and Fukuda, is directed to detecting soft error that may have accidentally occurred *during actual operation of the device*. A detection of an accidentally occurring soft error as in the claimed invention does not, in contrast to Shirasake and Fukuda, involve an external input to a memory, control of the memory, or addresses of the memory.

According to features in Claim 1, a compression circuit compresses information held in the information holding circuit, then expected value information is prepared separate from the compressed information, and a detecting circuit compares the expected value information with compression information of the information compression circuit to check for the destruction of information held in the information holding circuit. That is, in the claimed invention the detecting circuit detects corruption of information held in the information holding circuit, by comparing compressed information and expected value information.

The outstanding rejection is traversed as the admitted art does not disclose or suggest the above-noted operations or the claimed detecting circuit. Also, neither Shirasake nor Fukuda disclose or suggest such a detecting circuit, and thus Shirasake and Fukuda cannot cure the deficiencies of the admitted art in that respect. That is, no combination of the applied art fully meets all the claimed features of independent claim 1, and the claims dependent therefrom.

In view of these foregoing comments, applicant respectfully submits independent claim 1, and the claims dependent therefrom, distinguish over the admitted art in view of Shirasake and Fukuda.

With respect to the further independent claims 10, 14, and 18, applicant submits those claims also distinguish over the applied art.

The above-noted claims recite features of an “expected value correction circuit” and “a correction process execution circuit”. Those features are also directed to detecting a soft error that may have accidentally occurred *during an actual operation of a device*, again in contrast to Shirasake and Fukuda that relate to error detection performed *during testing of a memory*. The now independent claims 10, 14, and 18 also are directed to compressing information held in an information holding circuit, preparing expected value information separate from compressed information, and detecting corruption of information held in the information holding circuit by comparing the compressed information and the expected value information. Such features as discussed above are believed to clearly distinguish over the admitted art in view of Shirasake and Fukuda.

Moreover, no teachings in Kang or Whetsel are believed to cure the above-discussed deficiencies of the admitted art in view of Shirasake and Fukuda.

Kang is merely directed to detecting errors in data transmission. In Kang after data is transmitted and held in a register the device in Kang cannot detect whether or not data in the register has been corrupted. Thus, Kang does not provide any disclosures that would cure the above-discussed deficiencies of the admitted art in view of Shirasake and Fukuda.

Whetsel merely describes an IP macro and also does not provide any teachings that would cure the above-noted deficiencies of the admitted art in view of Shirasake and Fukuda.

In view of these foregoing comments, applicant respectfully submits the claims as written distinguish over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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